ABSTRACT OF THE DISCLOSURE

Disclosed is a method of forming a copper wiring in a semiconductor device. A copper barrier metal layer and a copper seed layer are sequentially formed along the surface of an interlayer insulating film including damascene patterns. In a state that a wafer is then loaded onto an electrical plating apparatus in which a copper plating solution is filled and a negative (-) power supply is also applied to the wafer, copper is plated so that the damascene patterns are sufficiently filled, thereby forming a copper layer. Next, the copper layer is polished in the plating solution by means of the electro-polishing process by changing the negative (-) power supply to the positive (+) power supply. Due to this, the surface of the copper layer is flat over the entire wafer. Thereafter, a chemical mechanical polishing process is performed until the surface of the interlayer insulating film is exposed, thereby forming copper wirings within the damascene patterns. As such, an uneven surface of the copper layer plated by the electroplating method is etched in the plating solution, thus making flat the surface of the copper layer and thin the thickness of the copper layer. It is thus possible to prevent a dishing phenomenon or an erosion phenomenon in a subsequent chemical mechanical polishing process. Therefore, the process margin of the chemical mechanical polishing process could be increased and process characteristics could be improved.